# EV182656558

#23/12-20-02

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applied tion Serial No. 09/332,271
Hilling Date June 11, 1999
Inventor Klaus Florian Schuegraf et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Ron E. Pompey
Attorney's Docket No. MI22-532
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

#### SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether any of the submitted references is prior art. Copies of the references are attached.

Respectfully Submitted:

Dated: 12-13-02

D. Brent Kenady Reg. No. 40,045

TECHNOLOGY CENTER 2002

# UNITED STATES PATENT AND TRADEMARK OFFICE

Filing Date ..... June 11, 1999 Assignee . . . . . . Micron Technology, Inc. Examiner ...... Ron E. Pompey Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,

and Wordline, Transistor Gate, and Conductive Interconnect Structures

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Respectfully Submitted:

Dated: 5-6-02

D. Brent Kenady Reg. No. 40,045



# UNITED STATES PATENT AND TRADEMARK OFFICE

Applic	ation Serial No.		 
Filing	Date		 June 11, 1999
Inven	tor	. <i>.</i>	 . Klaus Florian Schuegraf et al.
Assig	nee	. <i></i>	 Micron Technology, Inc.
Group	Art Unit		 2812
Exam	iner	·	 Ron E. Pompey
			MI22-532
			and Conductive Interconnects.
			terconnect Structures

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Respectfully Submitted:

Dated: 3-13-02

D. Brent Kenady Reg. No. 40,045

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### SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

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Respectfully Submitted:

Dated: 2-7-02

D. Brent Kenady Reg. No. 40,045

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# EL355818248

Inventor:	Klass Florian Schuegraf et al.
Title:	Methods For Forming Wordlines, Transistor Gates, And Conductive
	Interconnects, And Wordline, Transistor Gate, and Conductive
	Interconnect Structures
Assignee:	Micron Technology, Inc.
	INFORMATION DISCLOSURE STATEMENT
The I	Examiner's attention is directed to the references listed on the attached
Form PTO-1	1449 and copies of which are attached.
Citati	ion of these references are respectfully requested.
Date:	Respectfully submitted,  Attorney: David G. Latwesen, Ph.D.
	Reg. No. 38,533
Date:	Inventor: Klaus Florian Schuegraf
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Date: 5/24/99

Inventor: Randhin P & Testing

Randhir P. S. Thakur

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(Use several sees if necessary) MI22-532 Form PTO-1449 U.S. DEPARTMENT OF COMMERCE SERIAL NO. PATENT AND TRADEMARK OFFICE Unknown Klaus Florian Schuegraf et al. FILING DATE GROUP Filed herewith Unknown U.S. PATENT DOCUMENTS \*Examiner Document Date Name Class Subclass Filing Date Initial Number If Appropriate 5,425,392 06/95 Thakur et al. ABAC AD ΑE ΑF AGAHΑI AJ ΑK FOREIGN PATENT DOCUMENTS Document Date Country Class Subclass Translation Number No AL OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) AK Taishi Kubota et al.; "The Effect of the Floating Gate/Tunnel SiO; Interface on FLASH Memory Data Retention Reliability"; 1994; 2 pages AL Shoue Jen Wang et al.: "Effects of Poly Depletion on the Estimate of Thin Dielectric Lifetime"; IEEE Electron Device Letters, Vol. 12, No. 11, November 1991; pp. 617-619 AMKlaus F. Schuegraf et al.; "Impact of Polysilicon Depletion in Thin Oxide MOS Technology"; 1993; pp. 86-88 E E. H. Snow et al.; "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon"; Journal of the Electrochemical ANSociety, March 1966; pp. 263-269 П **EXAMINER** DATE CONSIDERED \*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance aits not conformance with MPEP 609. Include copy of this form with next communication to applicant. 2800